

Atty. Dkt. No. 039153-0363 (F0804)

**REMARKS**

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.

After amending the claims as set forth above, Claims 1-20 have been restricted. Claims 15, 16 and 19 have been amended. No new matter is added. Accordingly, Claims 1-20 remain pending in this application.

In paragraphs 1-7 of the Office Action, the Examiner has restricted the claim invention into Group I, Claims 1-14, drawn to a method of forming integrated circuit by forming a second trench smaller/narrower than the first trench; and Group II, Claims 15-20 drawn to a method of forming a gate conductor for integrated circuit by using RELACS process for forming an aperture. Applicants hereby elect Group I and have amended Claims 15-20 to be drawn to the method of Group I. Accordingly, withdrawal of the restriction requirement is respectfully requested. Applicants reserve the right to prepare a divisional application on the subject matter of Group II.

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date

11-4-02

By

Joseph N. Ziebert

FOLEY & LARDNER  
777 East Wisconsin Avenue  
Milwaukee, Wisconsin 53202-5367  
Telephone: (414) 297-5768  
Facsimile: (414) 297-4900

Joseph N. Ziebert  
Attorney for Applicant  
Registration No. 35,421

**FAX COPY RECEIVED**

NOV 04 2002

Atty. Dkt. No. 039153-0363 (F0804)

## MARKED UP VERSION SHOWING CHANGES MADE

Below are the marked up amended claim(s):

1           15.    (Amended)   A method of manufacturing a gate conductor for an  
2   integrated circuit, the method comprising:

3                    providing a first layer above a gate dielectric layer, the gate dielectric  
4   layer being above a substrate, the first layer including silicon oxynitride or silicon rich  
5   nitride;

6                    providing a second layer above the first layer;

7                    forming a first aperture in the second layer;

8                    forming [an] a second aperture in the first layer utilizing a RELACS  
9   process, the second aperture being narrower than the first aperture;

10                   filling the first aperture and the second aperture with a gate conductor  
11   material; and

12                   removing the gate conductor material above the [first] second layer.

1           16.    (Amended)   The method of claim 15, [further comprising:] wherein

2                    [providing] the second layer is an oxide layer [above the first layer and  
3   forming an aperture in the oxide layer before forming the aperture in the first layer].

1           19.    (Amended)   The method of claim 16, wherein the gate conductor  
2   material is [also provided in the aperture in the oxide layer] silicided.